**ECEN 248 - Lab Report**

**Lab Number: 9**

**Lab Title: An Introduction to High-Speed Addition**

**Section Number: 519**

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**Date: 11/15/23**

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**Objectives:**

The purpose of this lab is to introduce a fast-adder circuit, called the carry-lookahead addition. Using a combination of structural and dataflow Verilog to design and simulate this adder. This lab builds on a previous lab in which propagation delay affects ripple-carry adder, preventing it from being appropriate for high-speed arithmetic units.

**Design:**

Before implementing a 4-bit carry-lookahead adder, a few sub-modules need to be created. First the Generate/Propagate Unit, then the carry lookahead unit, and finally the summation unit. Use the starter code provided in the prelab portion of the lab manual. These three submodules can be written using dataflow Verilog. All of the submodules need to design the 4-bit carry lookahead adder, create a new project, and add the three submodules source into the design source section of the project. Create a new design source for the 4-bit cacarry-lookaheaddder. Call on the 3 submodules written earlier and use the starter code provided in the prelab to complete this module.

Set the 4-bit carry lookahead module as the top, and add its test bench file ‘cla\_4bit\_tb.v’ into the simulation sources of the project. Run a behavioral simulation, to generate a waveform and ensure all tests have passed.

Once the simulation is successful, implement propagation delay. Starting with 2 ns gate-delays. Then in the test bench file modify the pre-made loop delay from 10 to a low value of 6. Re-simulate the project, and increase the gate delays and test bench loop delay by 1 ns until all tests pass in the simulation. This will be the final delay measurement.

Design a two-level carry-lookahead adder to add 16-bit numbers. To start, create a block\_carry\_lookahead\_unit module. Using the carry lookahead unit design in the prelab as a starting point complete this module.

Expand the Generate/Propagate and Summation units to 16 bits, and remove the gate-delays from all submodules. Combine these submodules with the new block carry module, implement the 16-bit carry-lookahead adder, and add the design sources of the project. Copy the test bench file associated with this module ‘cla\_16bit\_tb.v’ into the simulation sources of the project. Set these two sources as top of the design and simulation sources, and simulate.

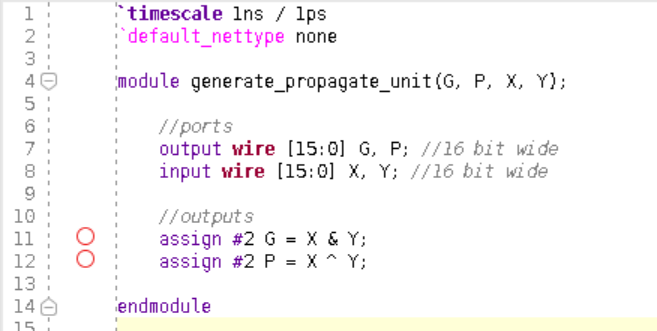
Once the simulation passes all the tests reincorporate the 2 ns gate-delays to the submodules and set the **TEST\_DELAY define** in the test bench file to the block\_carry\_lookahead\_unit delay. Resimulate and decrement the **TEST\_DELAY** and resimulate until some test fails.

**Conclusion:**

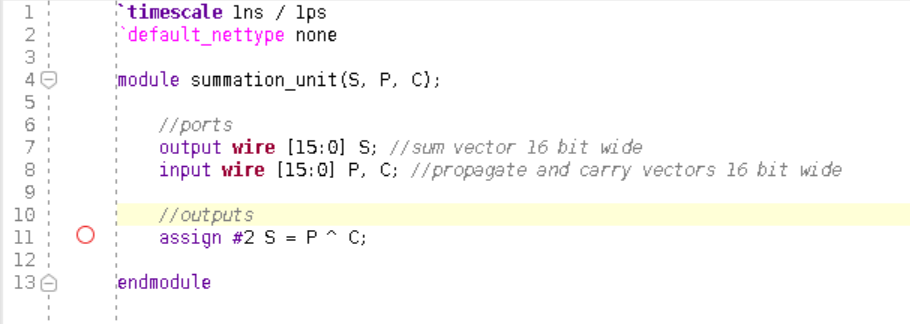
In this lab, I was able to design a two-level carry-lookahead adder and was able to see the benefits of using a carry-lookahead adder vs a ripple carry adder for large designs.

**Post-lab Deliverables:**

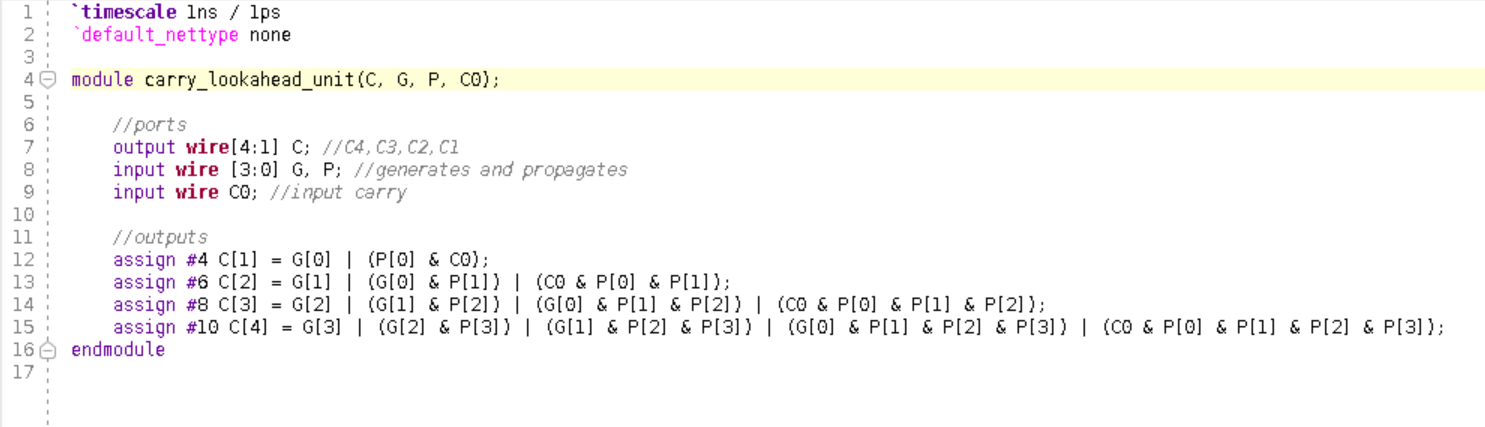
1. **Source code**



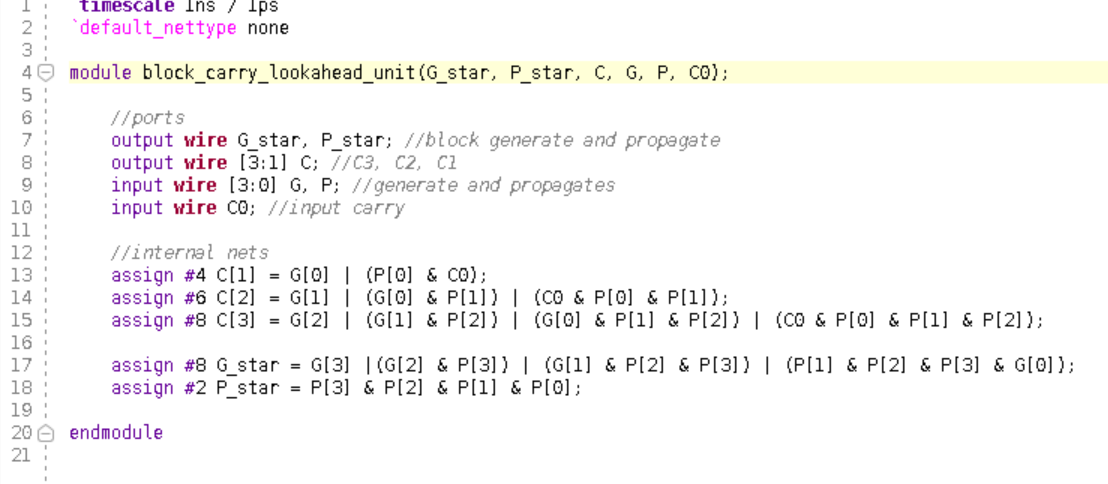
**Figure 1: GPU Code**

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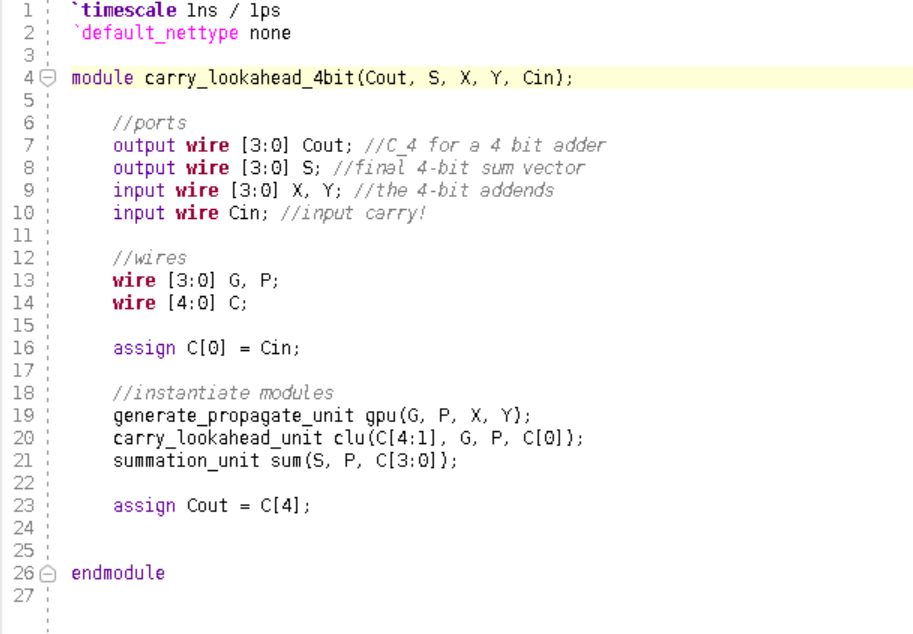
**Figure 2: Summation Unit Code**

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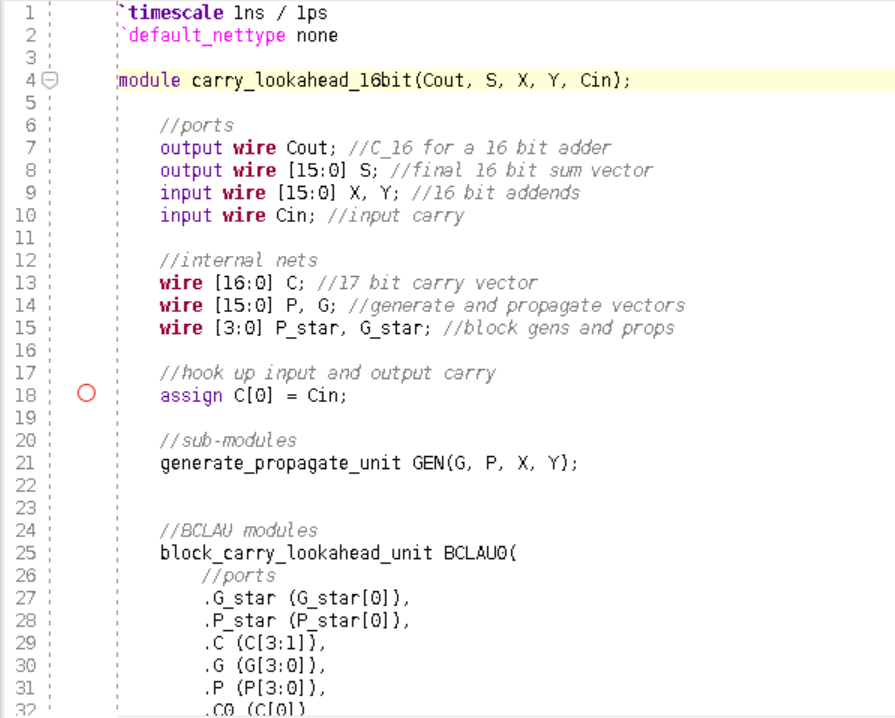
**Figure 3: Carry Lookahead Unit Code**

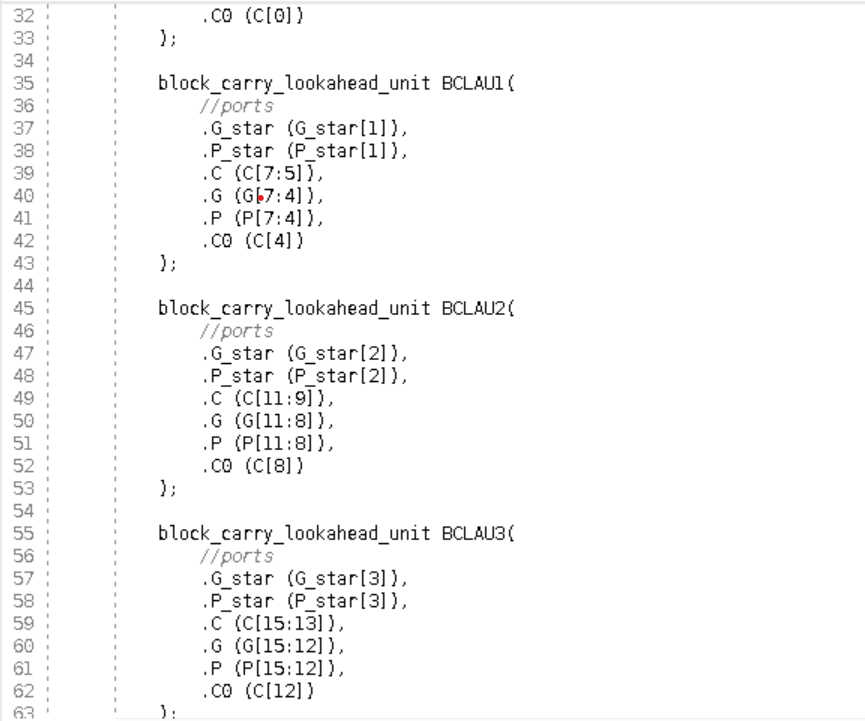
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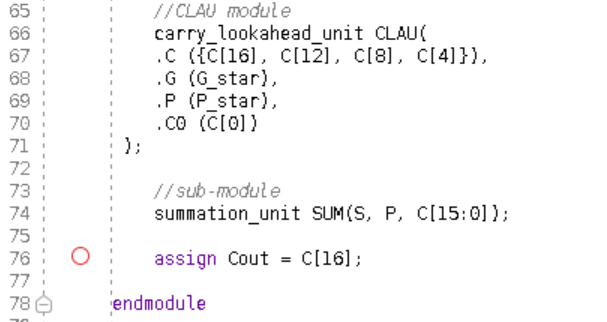
**Figure 4: Block Carry Lookahead Unit Code**

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**Figure 5: Carry Lookahead 4-bit Code**

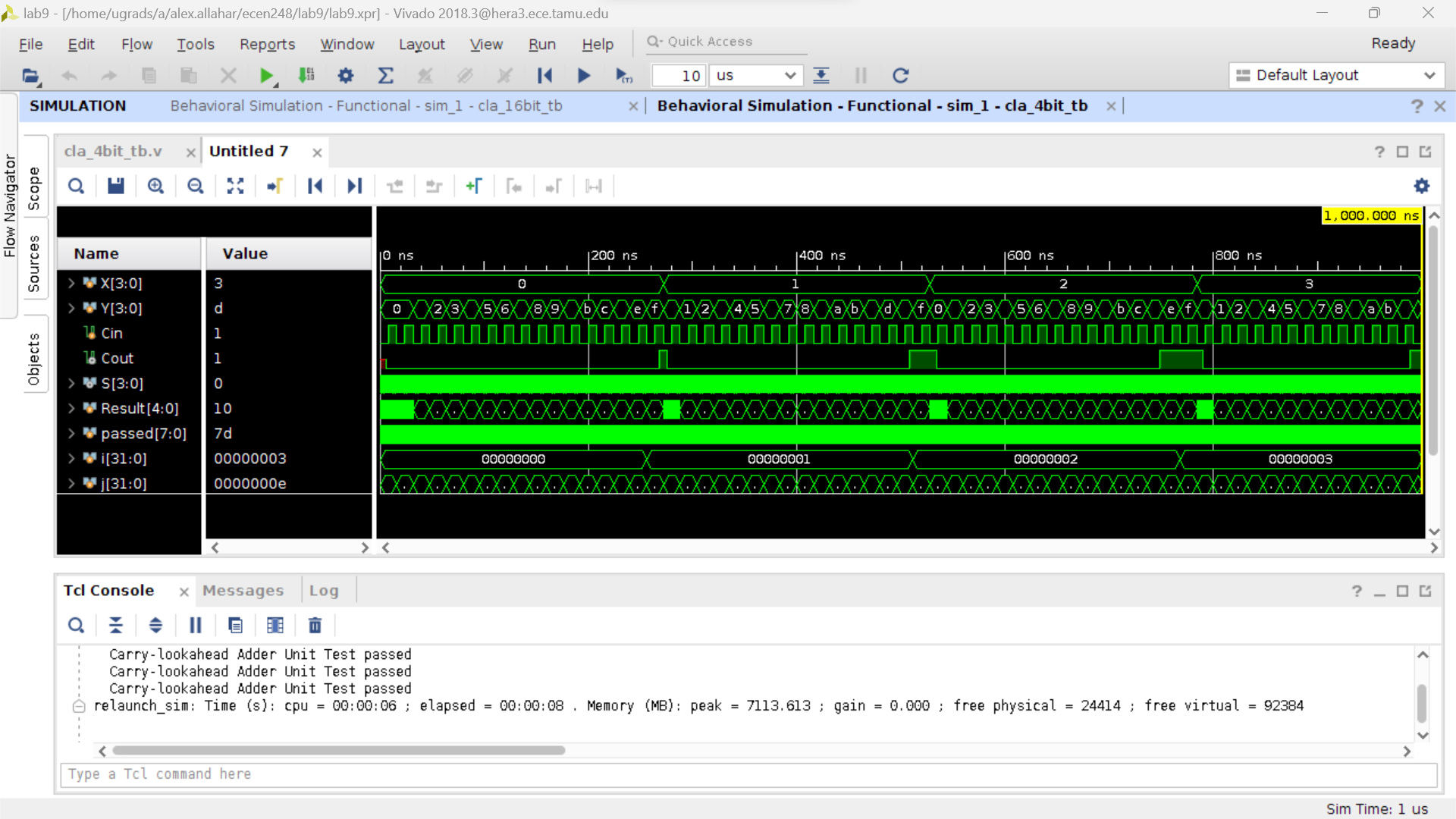
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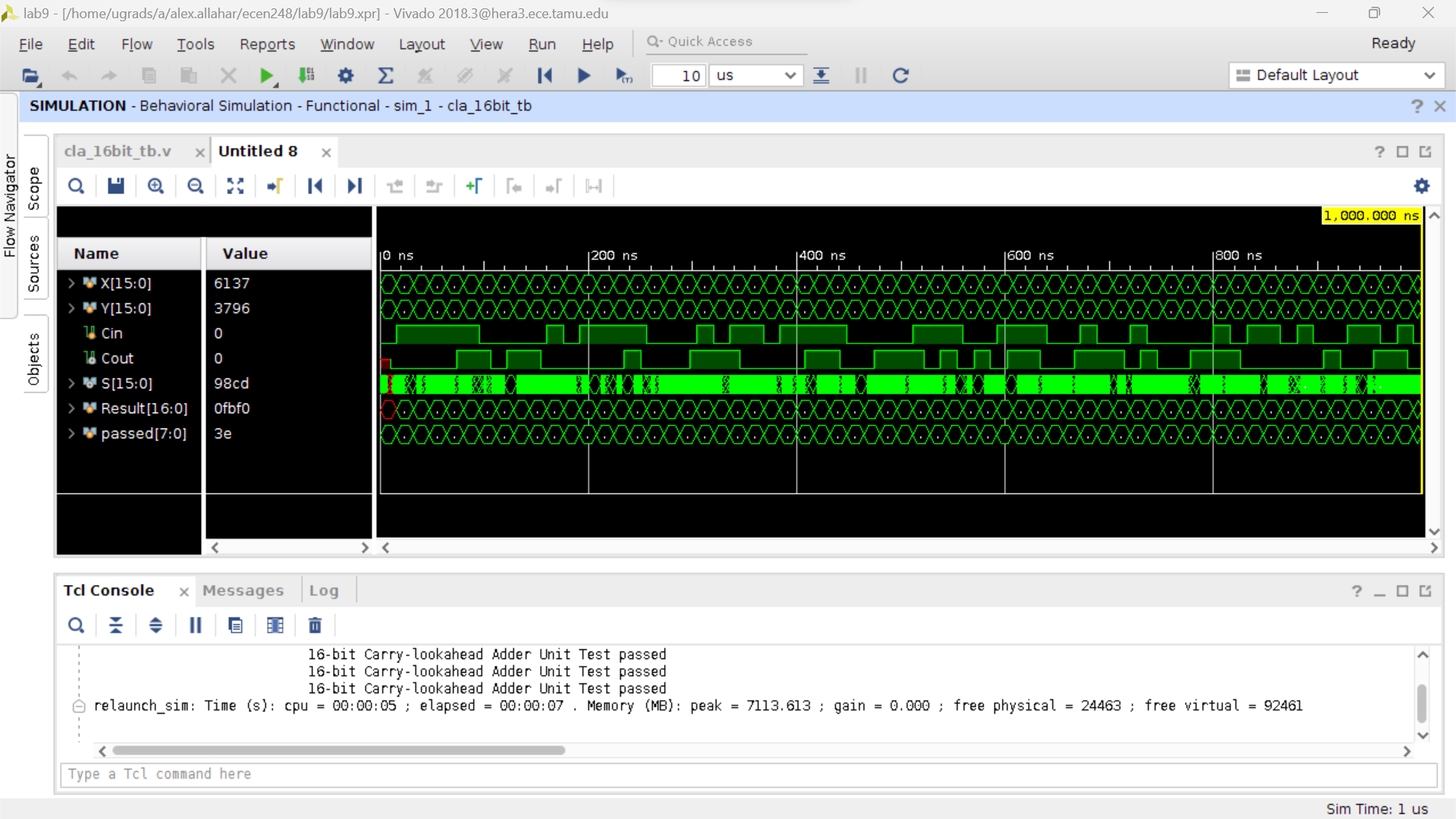
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**Figure 6: Carry Lookahead 16 bit Code**

1. **Simulation screenshots**

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**Figure 7: 4-bit Lookahead with delay**

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**Figure 8: 16 bit Lookahead with delay**

1. **Questions**
   1. Final Delay = 34 gates
   2. Propagation Delay = 16 ns
   3. Does the Delay match?
2. How does the gate-count of the 16-bit carry-lookahead adder compare to that of a ripple-carry adder of the same size? Give gate counts for both.

A 16-bit carry lookahead adder has 216 gates; whereas, a ripple-carry adder has 30 gates. The 16-bit carry lookahead adder has more gates than the ripple-carry adder, but is faster.

1. How does the propagation delay of the 4-bit carry-lookahead adder compare to that of a ripple-carry adder of the same size? Give delay values for both.

The 4-bit carry lookahead adder has 4 gate delays, and the 4-bit ripple carry adder has 9 gate delays.

1. Similarly, how does the propagation delay of the 16-bit carry-lookahead adder compare to that of a ripple-carry adder of the same size? Give delay values for both.

The 16-bit carry-lookahead adder has 8 gate delays, and the 16-bit ripple-carry adder has 34 gate delays.

1. Compare the delay growth of a ripple-carry adder versus a carry-lookahead adder. (ie. How does the delay increase as we increase the size of each adder?

The delay growth of a ripple-carry adder is 2n+1; whereas, the delay of the carry-lookahead is log(base4)(n)\*levels. The delayed growth of the carry-lookahead is much smaller than the ripple-carry adder.